

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Mukesh K Patel Examiner: Chameli C. Das
Serial No.: 09/687,777 Group Art Unit: 2122
Filed: 10/13/2000 Docket: 000006.P001X
Title: Java Hardware Accelerator Using Microcode Engine

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. § 1.97(c)(2), a check for the fee of \$180.00 as set forth in 37 C.F.R. § 1.17(p) is enclosed. Authorization is hereby given to charge any additional fees, or to credit any overpayment to Deposit Account No. 503437.

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

MUKESH K PATEL

By his Representatives,

Hahn and Moodley LLP

05/10/2005 SSESHE1 0000061 09687777
02 FC:1806 180.00 0P

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Serial No. 09/687,777

Filing Date: No

Title: Java Hardware Accelerator Using Microcode Engine

Page 2

Dkt: 000006.P001X

Suite 180, 800 W El Camino Real
Mountain View
CA 94040
Tel. No. 650 903 2257

Date May 5, 2005

By 
Vani Moodley
Reg. No. 56631

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313 1450, on this 5/11 day of May, 2005.

Name

VANI MOODLEY

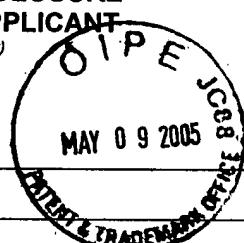
Signature



Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Complete if Known

Application Number	09/687,777
Filing Date	October 13, 2000
First Named Inventor	Patel, Mukesh
Group Art Unit	2122
Examiner Name	Das, Chameli

Sheet 1 of 1

Attorney Docket No: 000006.P001X

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US-6,003,038	12/14/1999	Chen, Tao S., et al.	
	US-6,065,108	05/16/2000	Tremblay, Mark , et al.	
	US-6,275,903	08/14/2001	Koppala, Sailendra , et al.	
	US-6,292,883	09/18/2001	Augustijn, Alexander , et al.	
	US-6,317,872	11/13/2001	Gee, John K., et al.	
	US-6,321,323	11/20/2001	Nugroho, Sofyan I., et al.	
	US-6,330,659	11/12/2001	Poff, Thomas C., et al.	
	US-6,374,286	04/16/2002	Gee, John K., et al.	
	US-6,532,531	03/11/2003	O' Conner, Michael , et al.	
	US-6,606,743	08/12/2003	Raz, Yair , et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		ROSE, A C., "Hardware Java Accelerator for the ARM 7", <u>4th Year Undergraduate Project in Group D</u> , (1996/97), 1-49, Appendix	
		STEINBUSCH, OTTO , "Designing Hardware to Interpret Virtual Machine Instructions", Dept. of Electrical Engineering, Eindhoven University of Technology, Masters Degree Thesis, February 1998, 59	

EXAMINER**DATE CONSIDERED**